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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,732	02/13/2002	Leo Mathew	SC11805TP	6370

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MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY
LAW SECTION
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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,732	MATHEW ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Invention II, claims 1 - 25 in Paper No. 4 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Applicant's election of Species II, claims 1, 2, and 4 – 25 in Paper No. 7 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 2, 4, 11, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Adkisson et al. (USPAT 6472258, Adkisson).

With regard to claim 1, Adkisson discloses in figures 1 – 5 a method of forming a vertical double gate semiconductor device. Adkisson discloses in figure 1 providing a semiconductor substrate (10). Adkisson discloses in figure 1 providing a first insulating layer (12) over the semiconductor substrate. Adkisson discloses in figure 1 providing a first semiconductor layer (14) over the first insulating layer. Adkisson discloses in figures 1 and 2, and column 3, lines 3 – 37 removing portions of a first semiconductor layer to form the semiconductor structure having a first sidewall (left side of the middle Si region) and a second sidewall (right side of the middle Si region), wherein the first sidewall is opposite the second sidewall. Adkisson discloses in figure 2 forming a first current electrode region (region to the right of the first sidewall) and a second current electrode region (region to the left of the second sidewall) in the semiconductor substrate. Adkisson discloses in figure 2 forming a second insulating layer (gate oxide) adjacent the first sidewall and the second sidewall. Adkisson discloses in figure 2 and column 3, lines 40 – 49 forming a conductive layer (20) over the semiconductor structure and the second insulating layer. Adkisson discloses in figure 2 and column 3, lines 40 – 49 removing a portion of the conductive layer to form a first electrode region (to the left of the first sidewall) and a second electrode region (to the right of the second sidewall). Adkisson discloses in figure 2 wherein the first electrode region is adjacent the first sidewall of the semiconductor structure. Adkisson discloses in figure 2 wherein the second electrode region is adjacent the second sidewall of the semiconductor structure. Adkisson discloses in figure 2a the first electrode region and the second electrode region are physically isolated from each other.

With regard to claim 2, Adkisson discloses in figure 2 and column 3, lines30 – 36 wherein the semiconductor structure is a channel region of the vertical double gate semiconductor device.

With regard to claim 4, Adkisson discloses in figure 2 and column 3, lines 40 – 49 wherein removing the portions of the conductive layer comprises planarizing the conductive layer.

With regard to claim 11, Adkisson discloses in figure 3, figure 3a, figure 5, figure 5a, and column 3, line 61 – column 4, line 24 further comprising forming metal (liner and contacts) over the first electrode region and the second electrode region.

With regard to claim 16, Adkisson discloses in figure 3, and column 4, lines 20 – 24 wherein the metal is a stack of metal layers.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5 – 10, and 12 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson as applied to claims 1 and 11 above, and further in view of Fried et al. (USPUB 2003/0113970, Fried).

With regard to claims 5 and 6, Adkisson discloses in figure 2 and column 3, lines 41 – 48 wherein forming the conductive layer further comprises forming a second semiconductor layer (20). Adkisson discloses in figure 2 and column 3, lines 41 – 48 wherein the semiconductor layer is conductive. Adkisson does not teach doping the second semiconductor layer in a first area adjacent the semiconductor structure with a first species. Fried teaches in figure 2b, figure 3b, and paragraph 0031 doping a second semiconductor layer (18) in a first area (24) adjacent a semiconductor structure (12) with a first species (20). Fried further teaches in figure 3b and paragraph 0031 doping the second semiconductor layer in a second area (26) adjacent the semiconductor structure with a second species (22), wherein the second species is different than the first species and the second area is different than the first area. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the double doping process of Fried in the method of Adkisson in order to make the second semiconductor layer conductive and shift the threshold voltage of the device to be compatible with current state of the art CMOS technology as stated by Fried in paragraph 0007.

With regard to claim 7, Fried teaches in figure 3b and paragraph 0031 wherein doping the second semiconductor layer is performed by ion implantation at an angle relative to a top surface of the semiconductor substrate.

With regard to claim 8, Fried teaches in paragraph 0032 further comprising annealing the first electrode region and the second electrode region after doping the second semiconductor layer.

With regard to claim 9, Adkisson teaches in figure 2 and column 3, lines 41 – 49 removing a portion of the conductive layer. It is not clear if Adkisson and Fried teach wherein

removing a portion of the conductive layer is performed after doping the second semiconductor layer in a first area adjacent the semiconductor structure with a first species. It would have been obvious in the method of Adkisson and Fried that the conductive layer would be removed only after the doping because the second semiconductor of Adkisson is only referred to as gate material. An intrinsically deposited polysilicon would not be sufficient to act as a gate material of the device in Adkisson, and therefore must be made conductive by doping through the method of Fried.

With regard to claim 10, Fried discloses in figure 3b wherein the first area is part of the first electrode region and the second area is part of the second electrode region.

With regard to claim 12, Adkisson discloses in figure 5, and column 4, lines 14 – 23 wherein forming the metal comprises forming a silicon layer (layer of polysilicon in column 4, lines 20 – 21) over the first electrode region, the second electrode region, and the semiconductor structure. Adkisson discloses in figure 5, and column 4, lines 14 – 23 forming a first metal layer (silicide of column 4, line 14) over the silicon layer. Adkisson does not teach heating the semiconductor substrate so that the silicon layer and the first metal layer form a silicide. Salicide processing is a well known technique to form silicide layers. Fried teaches in figures 3b, figure 4b, and paragraph 0032 a salicide technique for forming silicide layers. Fried teaches in figures 3b, figure 4b, and paragraph 0032 wherein forming the forming a first metal layer over a silicon layer (28). Fried teaches in figures 3b, figure 4b, and paragraph 0032 heating the semiconductor substrate (10b) so that the silicon layer and the first metal layer form a silicide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the salicide process of Fried in the method of forming a silicide of Adkisson in order to create a

contact that has no abrupt electrical barrier between it and the electrode. Such a contact provides superior electrical connection as is well known in the art.

With regard to claim 13, Adkisson discloses in figure 3, figure 3b, and column 4, lines 16 – 17 removing a portion of the metal to form a first contact for the first electrode region and a second contact for the second electrode region, wherein the first contact and the second contact are electrically isolated from each other.

With regard to claim 14, Adkisson discloses in figures 5 and 5a and column 4, lines 65 – column 5, line 12 wherein removing a portion of the metal comprises planarizing (damascene and conventional contacts) the metal.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson as applied to claims 1 and 11 above, and further in view of Forbes et al. (USPAT 6414356, Forbes).

With regard to claim 15, Adkisson discloses in figures 2 – 3 forming first and second electrode regions before forming the metal. Adkisson does not teach further comprising annealing the first electrode region and the second electrode region before forming the metal. Forbes teaches in figure 4L, figure 4M, figure 5a, column 12, lines 35 – 55, and column 13, lines 16 – 61 annealing a first electrode region (463a) and a second electrode region (463b) before forming a metal (560). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the annealing of Forbes in the method of Adkisson in order to activate dopant species in the gate layer as stated by Forbes in column 12, lines 35 – 55.

8. Claims 17 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson in view of Fried.

With regard to claim 17, Adkisson discloses in figures 1 – 5 a method of forming a vertical double gate semiconductor device. Adkisson discloses in figure 1 providing a semiconductor substrate (10). Adkisson discloses in figure 1 forming a first insulating layer (12) over the semiconductor substrate. Adkisson discloses in figure 1 forming a first semiconductor layer (14) on the first insulating layer. Adkisson discloses in figures 1 and 2 etching portions of the first semiconductor layer to form a semiconductor structure (Si) having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall in a first direction. Adkisson discloses in figures 1 – 3a and column 2, lines 48 – 57 forming a source region and a drain region in the semiconductor substrate in a second direction, wherein the first direction is substantially perpendicular the second direction. Adkisson discloses in figure 2 forming a second insulating layer on the first sidewall and the second sidewall. Adkisson discloses in figure 2 and column 3, lines 40 – 49 forming a second semiconductor layer (20) over the semiconductor structure and the second insulating layer. Adkisson discloses in figure 2 and column 3, lines 41 – 49 wherein the second semiconductor layer comprises (before polishing and recessing steps disclosed in figure 3, lines 41 – 42) a first semiconductor portion which is adjacent the first sidewall, a second semiconductor portion which is over the semiconductor structure, and a third semiconductor portion which is adjacent the second sidewall. Adkisson discloses in figure 2, and column 3, lines 40 – 49 that the gate polysilicon is conductive in order for the device to be capable of working as a semiconductor device. Adkisson does not teach doping by an angular implant the first semiconductor portion and the third semiconductor portion. Fried discloses in

figure 3b, and paragraph 0031 doping by an angular implant (20 and 22) a first semiconductor portion (24) and a third semiconductor (26) portion. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the doping of Fried in the method of Adkisson in order to make the second semiconductor layer conductive and shift the threshold voltage of the device to be compatible with current state of the art CMOS technology as stated by Fried in paragraph 0007. Adkisson discloses in figure 2, and column 3, lines 40 – 49 removing the second semiconductor portion.

With regard to claim 18, Adkisson discloses in column 3, lines 37 - 40 wherein the second insulating layer is deposited conformally (deposited).

With regard to claim 19, Fried teaches in paragraph 0032 further comprising annealing the second semiconductor layer.

With regard to claim 20, Adkisson teaches in figure 2 and column 3, lines 41 – 49 removing the second semiconductor portion. It is not clear if Adkisson and Fried teach wherein removing the second semiconductor portion is performed after doping the second semiconductor layer. It would have been obvious in the method of Adkisson and Fried that the second semiconductor portion would be removed only after the annealing because the second semiconductor of Adkisson is only referred to as gate material. The deposited polysilicon of Fried would not be sufficient to act as a gate material of the device in Adkisson until the layer is conductive enough to be a gate polysilicon. Therefore, the gate polysilicon must be annealed in the method of Adkisson and Fried before removal of the second semiconductor portion because the annealing is part of forming the gate polysilicon.

With regard to claim 21, Adkisson discloses in column 3, lines 40 – 49 wherein removing the second portion is performed by planarization (polished).

With regard to claim 22, Fried teaches in figure 3b and paragraph 0031 wherein doping the first semiconductor portion and the third semiconductor portion further comprises doping the first semiconductor portion with a first species and doping the third semiconductor portion with a second species, wherein the first species and the second species are different in conductivity.

With regard to claim 23, Fried teaches in figure 3b and paragraph 0031 wherein doping the first semiconductor portion and the third semiconductor portion is performed by ion implanting species at an angle relative to a top surface of the semiconductor substrate.

With regard to claim 24, Fried teaches in figure 3b and paragraph 0031 wherein doping the first semiconductor portion and the third semiconductor portion further includes forming a patterned layer (14) over the semiconductor substrate.

With regard to claim 25, Adkisson discloses in figures 1 and 2; and column 3, lines 20 – 30 wherein etching portions of the first semiconductor layer to form the semiconductor structure further comprises: forming a third insulating layer (thin oxide) over the first semiconductor layer; forming a nitride layer (SiN) over the third insulating layer; patterning the nitride layer and the third insulating layer; and etching the first semiconductor layer using the nitride layer and the third insulating layer as a mask.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fried et al. '469, Forbes et al. '065, Krivokapic et al., Yu '662, Yu '182, and Schlosser et al. all disclose double gated devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II